PATENT ABSTRACTS OF JAPAN

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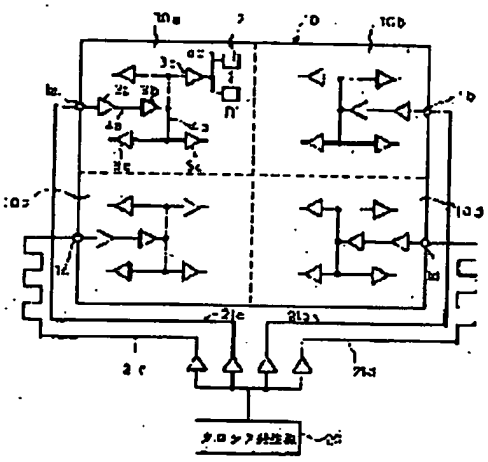
KOIDE KAZUO

(54) LOGICAL INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To provide a technique which can design a clock distribution system comparatively easily making a clock skew to be minimum.
CONSTITUTION: This circuit is designed by dividing a semiconductor chip 10 into the plural blocks 10a to 10d of which area are mostly equal one another, respectively/individually providing the clock distribution system including clock input terminals 1a to 1d, buffer circuits 3a to 3c and phase adjusting circuits for respective blocks and providing the clock distribution system in the shape of a tree for the respective blocks so that the wiring between respective nodes are equal in length and capacitance. Consequently, as the semiconductor 10 is divided into the plural blocks 10a to 10d, the wiring length from the clock input terminals 1a to 1d to flip-flops, etc., at ends become short so that the wiring designation of the equal length and capacity becomes easy, and a clock delay time from input terminals to the end circuits become short so that the absolute value of clock can be reduced.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is applied to a logic integration circuit technical pan at the supply system of a clock signal, especially, concerning an effective technique, is used for the distribution circuit of the clock signal in Logic LSI, and relates to an effective technique.
[0002]
[Description of the Prior Art] Conventionally, in Logic LSI, the whole LSI may be operated synchronizing with two or more clock signals with which one clock signal differs from a phase. In such a case, although the read/write of decoding or memory, various operations, etc. are operated by distributing the basic clock signal supplied from the outside to the flip-flop of each part in LSI etc., if the wire lengths from the distribution origin of a clock to a supply place differ, a gap (clock skew) will occur to the attainment timing of each clock. When there is clock skew, the signal mistaken by the flip-flop is incorporated, or there is a possibility that a non-wanted mustache-like pulse may occur in an output and a circuit may malfunction in a logic gate. Therefore, in the clock synchronous type LSI, the size of clock skew becomes the factor which opts for the engine performance (working speed) of LSI.
[0003] Then, conventionally, in order to make this clock skew into min, for example, as shown in drawing 6 , the clock input terminal 1 of LSI to the flip-flop 2 of an end prepares two or more buffer circuits 3a and 3b and 3c...., and connects the clock supply line 4 in the shape of a tree. That is, the technique of designing clock distributive system was adopted so that a clock might be made to distribute gradually like .... 8 times 4 times twice and the load-carrying capacity (wiring capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage might be in agreement (refer to "A Two-ChipCMOS64b Mainframe Processor Chipset"P [besides CICC'91 Mikio Yamagishi] - P).
[0004]
[Problem(s) to be Solved by the Invention] However, the clock skew in Logic LSI is produced according to various causes, such as fluctuation of the engine-performance variation of the transistor which constitutes not only the load-carrying capacity of each buffer circuit but a buffer circuit, or supply voltage, temperature variation, wiring capacity variation, gate capacitance variation, and wiring resistance variation. On the other hand, since LSI is in the formation of a large chip, and the inclination integrated highly increasingly in recent years, the distance from a clock input terminal to the flip-flop of an end etc. becomes still longer, and, moreover, wiring resistance becomes larger with detailed-izing of a pattern. Therefore, a clock time delay until it reaches the flip-flop of an end etc. from a clock input terminal becomes long, and minimization of the part clock skew becomes difficult. Therefore, when clock skew tended to design min clock distributive system by the above-mentioned conventional design technique, while the activity was very troublesome, it turned out that there is a trouble that a limitation is

generated naturally also in minimization of clock skew.
[0005] The purpose of this invention is to offer the design technique in which the clock distributive system which makes clock skew min comparatively simply is realizable. It will become clear [about the other purposes and the new description] from description and the appending drawing of this specification along [said] this invention.
[0006]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is explained among invention indicated in this application. Namely, while constituting independently clock distributive system including the buffer circuit which divided the inside of a semiconductor chip into two or more blocks with an almost equal area mutually, and was connected to a clock input terminal and this terminal for every block, respectively While preparing two or more steps of buffer circuits for every block, and constituting clock distributive system in the shape of [which branches gradually toward the end circuit of a clock supply place] a tree and becoming merits [wiring / between a stage and each buffer circuit], and the amount of isochore It is made to design so that the number of fan-outs of the buffer circuit of each stage may become the same.
[0007]
[Function] since the semiconductor chip is divided into two or more blocks -- the wire length from a clock input terminal to the flip-flop of an end etc. -- short -- becoming -- etc. -- while the wiring design of merit and the amount of isochore becomes easy, a clock time delay until it arrives at an end circuit from an input terminal becomes short, and can make the absolute value of clock skew small.
[0008]
[Example] One example of the clock distributive system in the logic LSI which applied this invention is shown in drawing 1 . In drawing 1 , the component from which 10 constitutes an integrated circuit, the semiconductor chip with which wiring is formed, and 1a, 1b, 1c, and 1d are the pads as a clock input terminal formed in the semiconductor chip 10. In this example, it is divided into the blocks 10a, 10b, 10c, and 10d of area [semiconductor chip / 10], and the above-mentioned clock input terminals 1a, 1b, 1c, and 1d are formed for every block.
[0009] And they are two or more buffer circuits 3a, 3b, and 3c for every block.... Cascade connection is carried out, the clock supply lines 4a and 4b and 4c.. are formed in the shape of a tree toward an end circuit, and twice, 4 times, the clock is constituted by this so that it may branch gradually and may be distributed like .. 8 times. And the number of fan-outs of the wire length between the flip-flops 2 as between buffer circuits and a limit buffer circuit, and an end circuit or the buffer circuit of each stage is determined so that the load-carrying capacity (wiring capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage may be in agreement. Furthermore, in this example, it is designed so that it may become merits [wiring / 21a-21d / to each above-mentioned clock input terminals 1a, 1b, 1c, and 1d], and the amount of isochore from the source 20 of clock generation on the substrate in which the above-mentioned semiconductor chip 10 is carried.
[0010] With the application of the design technique of the above-mentioned clock distributive system, the example of a configuration of the microcomputer chip as suitable logic LSI is shown in drawing 2 . the inside of a chip divides the microcomputer of this example into four blocks -- having -- **** -- block 10a -- the arithmetic logical operation

machine ALU, the floating point controller FCT, and arithmetic register CRG -- moreover, the multiplier controller MCT, a register file RGF, the multiplier array MRY, an address register ARG, and the translation lookaside buffer circuit ACB are arranged at block 10c, and barrel shifter BST and the data cache memory DCM are further arranged for the instruction queue IQ, instruction register IR, and instruction decoder IDC at block 10b at block 10d, respectively. And the clock input terminals 1a, 1b, 1c, and 1d are formed every [each blocks 10a, 10b and 10c and] 10d, and the buffer circuit 3 and the supply line 4 for clock distribution are formed by the method shown in drawing 1 , and it is constituted so that a clock signal may be supplied to the flip-flop and logic gate within each circuit block. In addition, 6a-6d are input-output-buffer circuits.

[0011] The 2nd example of the clock distributing system concerning this invention is shown in drawing 3 . Also in this example, a semiconductor chip is quadrisected and the clock input terminal 1, a buffer circuit 3, and wiring 4 are formed for every block. Only the configuration of the clock distributive system in one block 10a is shown in drawing 3 . The configuration of clock distributive system is the same as that of the example of drawing 1 . although a frequency is lower than clock signal CK inputted into the clock input terminal 1 other than the clock input terminal 1, while a deer is carried out, and the terminal 11 into which the clock CKr for reference with the same phase is inputted is formed in this example -- the first rank of clock distributive system -- the delay equalization circuit 31 which can adjust the amount of delay of a clock between buffer circuit 3a and buffer circuit 3b of the next step is connected. Moreover, a buffer circuit 13 is connected to the above-mentioned clock input terminal 11 for reference, and the clock CKr for reference is supplied to the phase comparator circuit 32 at least through this buffer circuit 13.

[0012] Furthermore, clock CK' outputted to the input terminal of another side of this phase comparator circuit 32 from buffer circuit 3e of the last stage of clock distributive system is supplied, phase contrast with the above-mentioned clock CKr for reference is detected, and the signal according to that difference is supplied to a control circuit 15. And the control circuit 33 is constituted so that the phase contrast of the clock CK' and the above-mentioned clock CKr for reference which are outputted from buffer circuit 3e of the last stage becomes zero and the above-mentioned delay equalization circuit 31 may be controlled. Even if a gap is in the phase of the clock CK inputted into the each blocks [10a, 10b, 10c, and 10d] clock input terminals 1a, 1b, 1c, and 1d in this example The phase of clock CK' which will be supplied to the end circuits 2, such as a flip-flop, if even the phase of the clock CKr for reference is firmly carried out even if the delay of the clock signal from a clock input terminal to the flip-flop of an end differs for every clock is made in agreement by the whole LSI. It can **.

[0013] The 3rd example of the clock distributing system concerning this invention is shown in drawing 4 . This example sets the input terminal 1 of Clock CK to one in a semiconductor chip 10. The clock CKr for reference inputted into the clock input terminal 11 for reference is transmitted to buffer circuit 13b in which it was once prepared in the center of a chip from buffer circuit 13a. It is made to supply with wiring of die length equal to the clock phase adjustment circuits 30a-30d prepared from there in each blocks 10a, 10b, and 10c and 10d. The clock phase adjustment circuits 30a-30d can constitute at least the delay equalization circuit 31 by the phase comparator circuit 32 and the control circuit 33 like the above-mentioned example.

[0014] Moreover, in this example, the clock CK inputted into the above-mentioned only clock input terminal 1 is supplied to each clock phase adjustment circuits 30a-30d in common. And within each block, like the above-mentioned example, cascade connection is carried out, the clock supply lines 4a and 4b and 4c.. are constituted in the shape of a tree, and clock CK' outputted from the clock phase adjustment circuits 30a-30d is distributed for two or more buffer circuits 3a and 3b and 3c.... to the flip-flop 2 grade of an end through buffer circuit 3b and 3c.. And the number of fan-outs of the wire length of the flip-flop 2 as between buffer circuits and a limit buffer circuit, and an end circuit or the buffer circuit of each stage is determined so that the load-carrying capacity (wiring capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage may be in agreement. In this example, even if a gap is in the phase of the clock inputted into the each blocks [10a, 10b, 10c, and 10d] clock phase adjustment circuits 30a-30d, since the phase of the clock CKr for reference is the same, the phase of clock CK' supplied to end circuits, such as a flip-flop, can be made in agreement by the whole LSI.
[0015] The example of 1 configuration of the above-mentioned delay equalization circuit 31 is shown in drawing 5 . Namely, while the above-mentioned delay equalization circuit 31 connects in juxtaposition two or more delay means D1, D2, and D3 which consist of the time constant circuit which has the respectively different amount of delay, or a logic-gate train, and ....Dn(s) The desired amount of delay is given by forming Selector SEL in the latter part, controlling Selector SEL by the control signal from a control circuit 33, and letting the delay means D1, D2, and D3 or ....Dn pass for clock signal CK from buffer circuit 3a.
[0016] In addition, although the above-mentioned example explained the case where a semiconductor chip was quadrisected If it is in the semiconductor chip of the so-called CCB mounting with which it comes to form a solder bump all over a chip Since a direct clock can be inputted into the interior of a chip and it can form in long [wiring / from the input terminal of a clock to each block / clock supply] wiring even if it does not consider as quadrisection like the above-mentioned example, a chip may be carried out to nine division or 16 division.
[0017] As explained above, the above-mentioned example divides the inside of a semiconductor chip into two or more blocks with an almost equal area mutually. And while constituting independently clock distributive system including the buffer circuit connected to a clock input terminal and this terminal for every block, respectively While preparing two or more steps of buffer circuits for every block, and constituting clock distributive system in the shape of [which branches gradually toward the end circuit of a clock supply place] a tree and becoming merits [wiring / between a stage and each buffer circuit], and the amount of isochore Since it was made to design so that the number of fan-outs of the buffer circuit of each stage may become the same the wire length from a clock input terminal to the flip-flop of an end etc. -- short -- becoming -- etc. -- while the wiring design of merit and the amount of isochore becomes easy, it is effective in the ability for the clock time delay from an input terminal to an end circuit to become short, and make the absolute value of clock skew small.
[0018] Although invention made by this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned example, and does not deviate from the summary. For example, although the above-mentioned example

explained taking the case of the case where the clock inputted is a plane 1, this invention is not limited to it, and also when two or more clocks with which phases differ mutually are inputted, it can be applied. In that case, what is necessary is just to design clock distributive system by the design technique of the above-mentioned example for every clock. However, in the example of drawing 3 or drawing 4 , the clock CKr for reference can be used in common to each clock. Although the above explanation explained the case where invention mainly made by this invention person was applied to the microcomputer which is a field of the invention used as that background, this invention is not limited to it and can be used for a general semi-conductor logic integration circuit.

[0019]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly. That is, it becomes possible to design comparatively simply the clock distributive system which makes clock skew min in Logic LSI.

TECHNICAL FIELD

[Industrial Application] This invention is applied to a logic integration circuit technical pan at the supply system of a clock signal, especially, concerning an effective technique, is used for the distribution circuit of the clock signal in Logic LSI, and relates to an effective technique.

PRIOR ART

[Description of the Prior Art] Conventionally, in Logic LSI, the whole LSI may be operated synchronizing with two or more clock signals with which one clock signal differs from a phase. In such a case, although the read/write of decoding or memory, various operations, etc. are operated by distributing the basic clock signal supplied from the outside to the flip-flop of each part in LSI etc., if the wire lengths from the distribution origin of a clock to a supply place differ, a gap (clock skew) will occur to the attainment timing of each clock. When there is clock skew, the signal mistaken by the flip-flop is incorporated, or there is a possibility that a non-wanted mustache-like pulse may occur in an output and a circuit may malfunction in a logic gate. Therefore, in the clock synchronous type LSI, the size of clock skew becomes the factor which opts for the engine performance (working speed) of LSI.

[0003] Then, conventionally, in order to make this clock skew into min, for example, as shown in drawing 6 , the clock input terminal 1 of LSI to the flip-flop 2 of an end prepares two or more buffer circuits 3a and 3b and 3c...., and connects the clock supply line 4 in the shape of a tree. That is, the technique of designing clock distributive system was adopted so that a clock might be made to distribute gradually like .... 8 times 4 times twice and the load-carrying capacity (wiring capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage might be in agreement (refer to "A Two-ChipCMOS64b Mainframe Processor Chipset"P [besides CICC'91 Mikio Yamagishi] -

P).

EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly. That is, it becomes possible to design comparatively simply the clock distributive system which makes clock skew min in Logic LSI.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the clock skew in Logic LSI is produced according to various causes, such as fluctuation of the engine-performance variation of the transistor which constitutes not only the load-carrying capacity of each buffer circuit but a buffer circuit, or supply voltage, temperature variation, wiring capacity variation, gate capacitance variation, and wiring resistance variation. On the other hand, since LSI is in the formation of a large chip, and the inclination integrated highly increasingly in recent years, the distance from a clock input terminal to the flip-flop of an end etc. becomes still longer, and, moreover, wiring resistance becomes larger with detailed-izing of a pattern. Therefore, a clock time delay until it reaches the flip-flop of an end etc. from a clock input terminal becomes long, and minimization of the part clock skew becomes difficult. Therefore, when clock skew tended to design min clock distributive system by the above-mentioned conventional design technique, while the activity was very troublesome, it turned out that there is a trouble that a limitation is generated naturally also in minimization of clock skew.
[0005] The purpose of this invention is to offer the design technique in which the clock distributive system which makes clock skew min comparatively simply is realizable. It will become clear [about the other purposes and the new description] from description and the appending drawing of this specification along [said] this invention.

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is explained among invention indicated in this application. Namely, while constituting independently clock distributive system including the buffer circuit which divided the inside of a semiconductor chip into two or more blocks with an almost equal area mutually, and was connected to a clock input terminal and this terminal for every block, respectively While preparing two or more steps of buffer circuits for every block, and constituting clock distributive system in the shape of [which branches gradually toward the end circuit of a clock supply place] a tree and becoming merits [wiring / between a stage and each buffer circuit], and the amount of isochore It is made to design so that the

number of fan-outs of the buffer circuit of each stage may become the same.

OPERATION

[Function] since the semiconductor chip is divided into two or more blocks -- the wire length from a clock input terminal to the flip-flop of an end etc. -- short -- becoming -- etc. -- while the wiring design of merit and the amount of isochore becomes easy, a clock time delay until it arrives at an end circuit from an input terminal becomes short, and can make the absolute value of clock skew small.

EXAMPLE

[Example] One example of the clock distributive system in the logic LSI which applied this invention is shown in drawing 1 . In drawing 1 , the component from which 10 constitutes an integrated circuit, the semiconductor chip with which wiring is formed, and 1a, 1b, 1c, and 1d are the pads as a clock input terminal formed in the semiconductor chip 10. In this example, it is divided into the blocks 10a, 10b, 10c, and 10d of area [semiconductor chip / 10], and the above-mentioned clock input terminals 1a, 1b, 1c, and 1d are formed for every block.

[0009] And they are two or more buffer circuits 3a, 3b, and 3c for every block.... Cascade connection is carried out, the clock supply lines 4a and 4b and 4c.. are formed in the shape of a tree toward an end circuit, and twice, 4 times, the clock is constituted by this so that it may branch gradually and may be distributed like .. 8 times. And the number of fan-outs of the wire length between the flip-flops 2 as between buffer circuits and a limit buffer circuit, and an end circuit or the buffer circuit of each stage is determined so that the load-carrying capacity (wiring capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage may be in agreement. Furthermore, in this example, it is designed so that it may become merits [wiring / 21a-21d / to each above-mentioned clock input terminals 1a, 1b, 1c, and 1d], and the amount of isochore from the source 20 of clock generation on the substrate in which the above-mentioned semiconductor chip 10 is carried.

[0010] With the application of the design technique of the above-mentioned clock distributive system, the example of a configuration of the microcomputer chip as suitable logic LSI is shown in drawing 2 . the inside of a chip divides the microcomputer of this example into four blocks -- having -- **** -- block 10a -- the arithmetic logical operation machine ALU, the floating point controller FCT, and arithmetic register CRG -- moreover, the multiplier controller MCT, a register file RGF, the multiplier array MRY, an address register ARG, and the translation lookaside buffer circuit ACB are arranged at block 10c, and barrel shifter BST and the data cache memory DCM are further arranged for the instruction queue IQ, instruction register IR, and instruction decoder IDC at block 10b at block 10d, respectively. And the clock input terminals 1a, 1b, 1c, and 1d are formed every [each blocks 10a, 10b and 10c and] 10d, and the buffer circuit 3 and the supply line 4 for clock distribution are formed by the method shown in drawing 1 , and it is constituted so that a clock signal may be supplied to the flip-flop and logic gate within

each circuit block. In addition, 6a-6d are input-output-buffer circuits.
[0011] The 2nd example of the clock distributing system concerning this invention is shown in drawing 3 . Also in this example, a semiconductor chip is quadrisected and the clock input terminal 1, a buffer circuit 3, and wiring 4 are formed for every block. Only the configuration of the clock distributive system in one block 10a is shown in drawing 3 . The configuration of clock distributive system is the same as that of the example of drawing 1 . although a frequency is lower than clock signal CK inputted into the clock input terminal 1 other than the clock input terminal 1, while a deer is carried out, and the terminal 11 into which the clock CKr for reference with the same phase is inputted is formed in this example -- the first rank of clock distributive system -- the delay equalization circuit 31 which can adjust the amount of delay of a clock between buffer circuit 3a and buffer circuit 3b of the next step is connected. Moreover, a buffer circuit 13 is connected to the above-mentioned clock input terminal 11 for reference, and the clock CKr for reference is supplied to the phase comparator circuit 32 at least through this buffer circuit 13.
[0012] Furthermore, clock CK' outputted to the input terminal of another side of this phase comparator circuit 32 from buffer circuit 3e of the last stage of clock distributive system is supplied, phase contrast with the above-mentioned clock CKr for reference is detected, and the signal according to that difference is supplied to a control circuit 15. And the control circuit 33 is constituted so that the phase contrast of the clock CK' and the above-mentioned clock CKr for reference which are outputted from buffer circuit 3e of the last stage becomes zero and the above-mentioned delay equalization circuit 31 may be controlled. Even if a gap is in the phase of the clock CK inputted into the each blocks [10a, 10b, 10c, and 10d] clock input terminals 1a, 1b, 1c, and 1d in this example The phase of clock CK' which will be supplied to the end circuits 2, such as a flip-flop, if even the phase of the clock CKr for reference is firmly carried out even if the delay of the clock signal from a clock input terminal to the flip-flop of an end differs for every clock is made in agreement by the whole LSI. It can **.
[0013] The 3rd example of the clock distributing system concerning this invention is shown in drawing 4 . This example sets the input terminal 1 of Clock CK to one in a semiconductor chip 10. The clock CKr for reference inputted into the clock input terminal 11 for reference is transmitted to buffer circuit 13b in which it was once prepared in the center of a chip from buffer circuit 13a. It is made to supply with wiring of die length equal to the clock phase adjustment circuits 30a-30d prepared from there in each blocks 10a, 10b, and 10c and 10d. The clock phase adjustment circuits 30a-30d can constitute at least the delay equalization circuit 31 by the phase comparator circuit 32 and the control circuit 33 like the above-mentioned example.
[0014] Moreover, in this example, the clock CK inputted into the above-mentioned only clock input terminal 1 is supplied to each clock phase adjustment circuits 30a-30d in common. And within each block, like the above-mentioned example, cascade connection is carried out, the clock supply lines 4a and 4b and 4c.. are constituted in the shape of a tree, and clock CK' outputted from the clock phase adjustment circuits 30a-30d is distributed for two or more buffer circuits 3a and 3b and 3c.... to the flip-flop 2 grade of an end through buffer circuit 3b and 3c.. And the number of fan-outs of the wire length of the flip-flop 2 as between buffer circuits and a limit buffer circuit, and an end circuit or the buffer circuit of each stage is determined so that the load-carrying capacity (wiring

capacity, input capacitance of the next step gate, etc.) of the buffer circuit of each stage may be in agreement. In this example, even if a gap is in the phase of the clock inputted into the each blocks [10a, 10b, 10c, and 10d] clock phase adjustment circuits 30a-30d, since the phase of the clock CKr for reference is the same, the phase of clock CK' supplied to end circuits, such as a flip-flop, can be made in agreement by the whole LSI.
[0015] The example of 1 configuration of the above-mentioned delay equalization circuit 31 is shown in drawing 5 . Namely, while the above-mentioned delay equalization circuit 31 connects in juxtaposition two or more delay means D1, D2, and D3 which consist of the time constant circuit which has the respectively different amount of delay, or a logic-gate train, and ....Dn(s) The desired amount of delay is given by forming Selector SEL in the latter part, controlling Selector SEL by the control signal from a control circuit 33, and letting the delay means D1, D2, and D3 or ....Dn pass for clock signal CK from buffer circuit 3a.
[0016] In addition, although the above-mentioned example explained the case where a semiconductor chip was quadrisected If it is in the semiconductor chip of the so-called CCB mounting with which it comes to form a solder bump all over a chip Since a direct clock can be inputted into the interior of a chip and it can form in long [wiring / from the input terminal of a clock to each block / clock supply] wiring even if it does not consider as quadrisection like the above-mentioned example, a chip may be carried out to nine division or 16 division.
[0017] As explained above, the above-mentioned example divides the inside of a semiconductor chip into two or more blocks with an almost equal area mutually. And while constituting independently clock distributive system including the buffer circuit connected to a clock input terminal and this terminal for every block, respectively While preparing two or more steps of buffer circuits for every block, and constituting clock distributive system in the shape of [which branches gradually toward the end circuit of a clock supply place] a tree and becoming merits [wiring / between a stage and each buffer circuit], and the amount of isochore Since it was made to design so that the number of fan-outs of the buffer circuit of each stage may become the same the wire length from a clock input terminal to the flip-flop of an end etc. -- short -- becoming -- etc. -- while the wiring design of merit and the amount of isochore becomes easy, it is effective in the ability for the clock time delay from an input terminal to an end circuit to become short, and make the absolute value of clock skew small.
[0018] Although invention made by this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned example, and does not deviate from the summary. For example, although the above-mentioned example explained taking the case of the case where the clock inputted is a plane 1, this invention is not limited to it, and also when two or more clocks with which phases differ mutually are inputted, it can be applied. In that case, what is necessary is just to design clock distributive system by the design technique of the above-mentioned example for every clock. However, in the example of drawing 3 or drawing 4 , the clock CKr for reference can be used in common to each clock. Although the above explanation explained the case where invention mainly made by this invention person was applied to the microcomputer which is a field of the invention used as that background, this invention is not limited to it

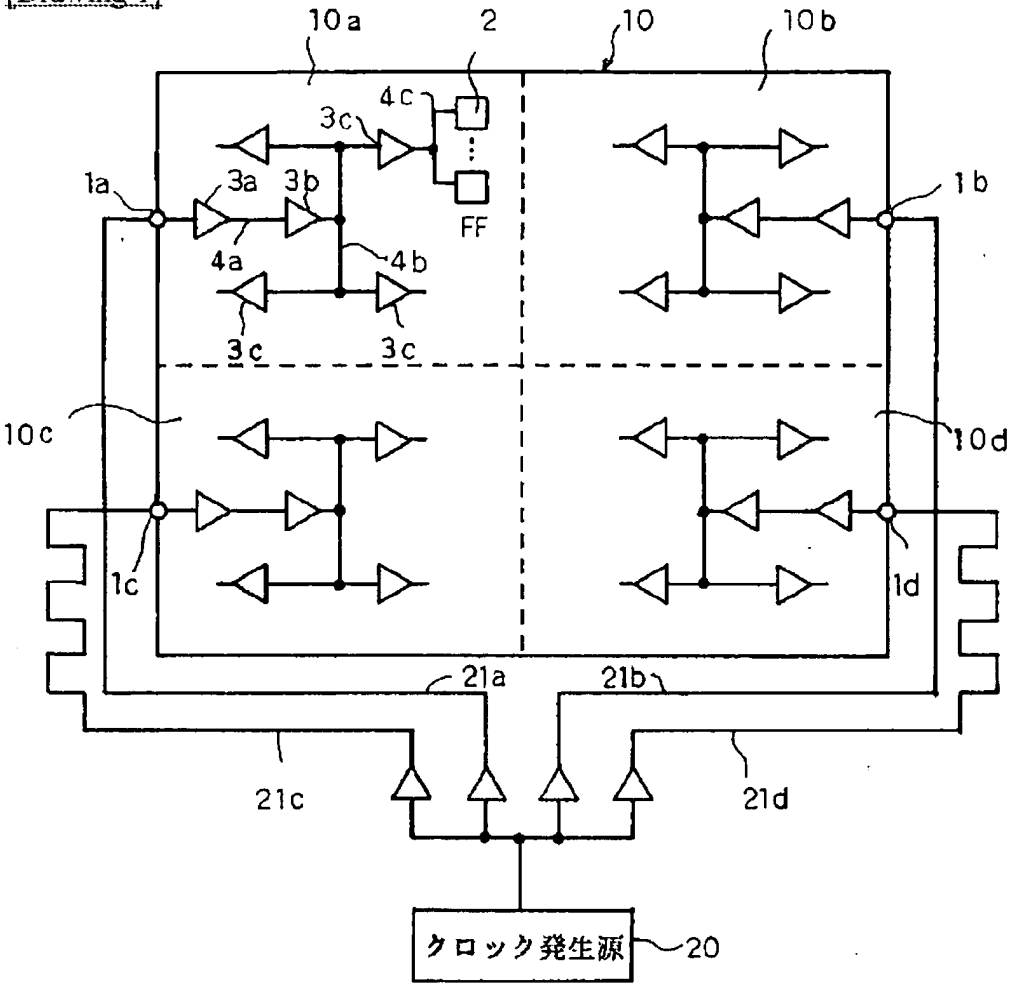
and can be used for a general semi-conductor logic integration circuit.

DESCRIPTION OF DRAWINGS

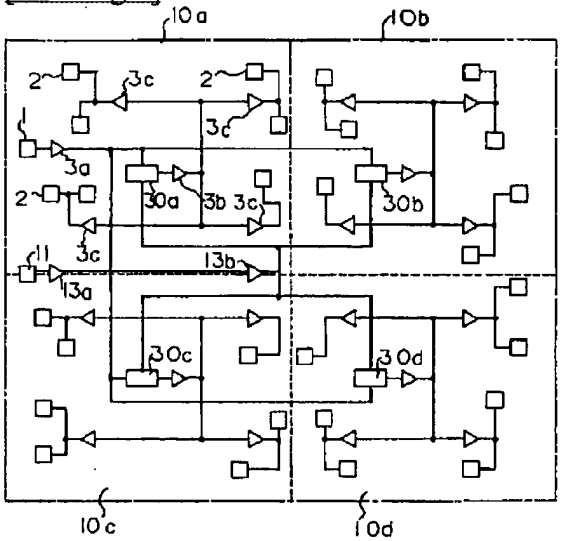
[Brief Description of the Drawings]
[Drawing 1] It is the circuitry Fig. showing one example of the clock distributive system in the logic LSI which applied this invention.
[Drawing 2] It is the block diagram showing the example of a configuration of the microcomputer chip as suitable logic LSI with the application of the design technique of the above-mentioned clock distributive system.
[Drawing 3] It is the circuitry Fig. showing the 2nd example of the clock distributive system in the logic LSI which applied this invention.
[Drawing 4] It is the circuitry Fig. showing the 3rd example of the clock distributive system in the logic LSI which applied this invention.
[Drawing 5] It is the circuitry Fig. showing the example of 1 configuration of the delay equalization circuit in drawing 3 and the drawing 4 logic integration circuit.
[Drawing 6] It is the circuitry Fig. showing an example of the conventional clock distribution circuit.
[Description of Notations]
1a, 1b, 1c, 1d Clock input terminal (pad)
2 End Circuit (Flip-flop)
3a, 3b, 3c Buffer circuit
4a, 4b, 4c Clock supply line
10 Semiconductor Chip
10a, 10b, 10c, 10d Block
30 Phase Adjustment Circuit
31 Delay Equalization Circuit

DRAWINGS

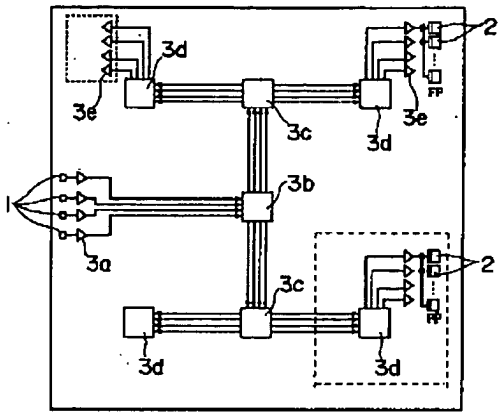
[Drawing 1]



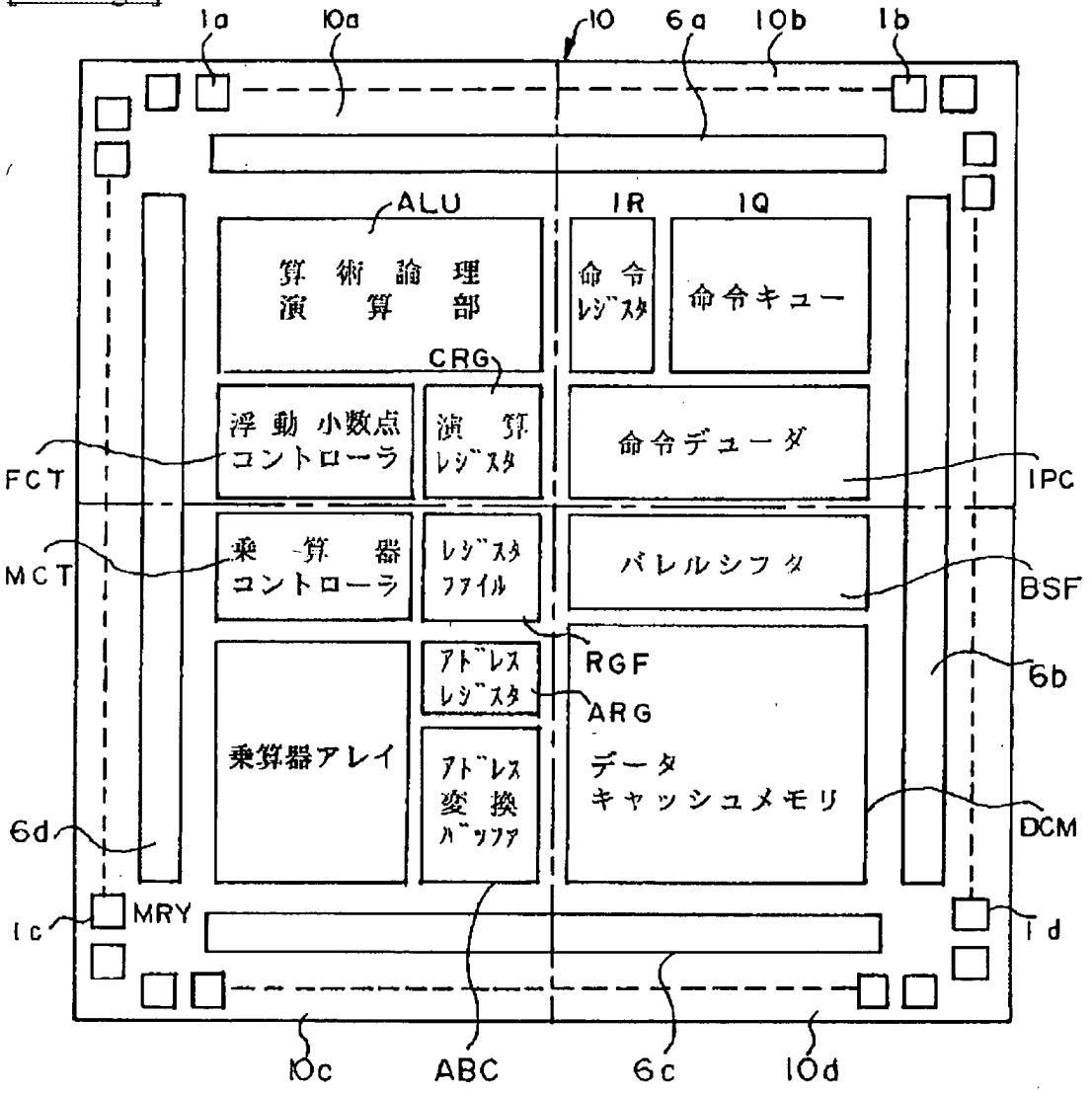
[Drawing 4]



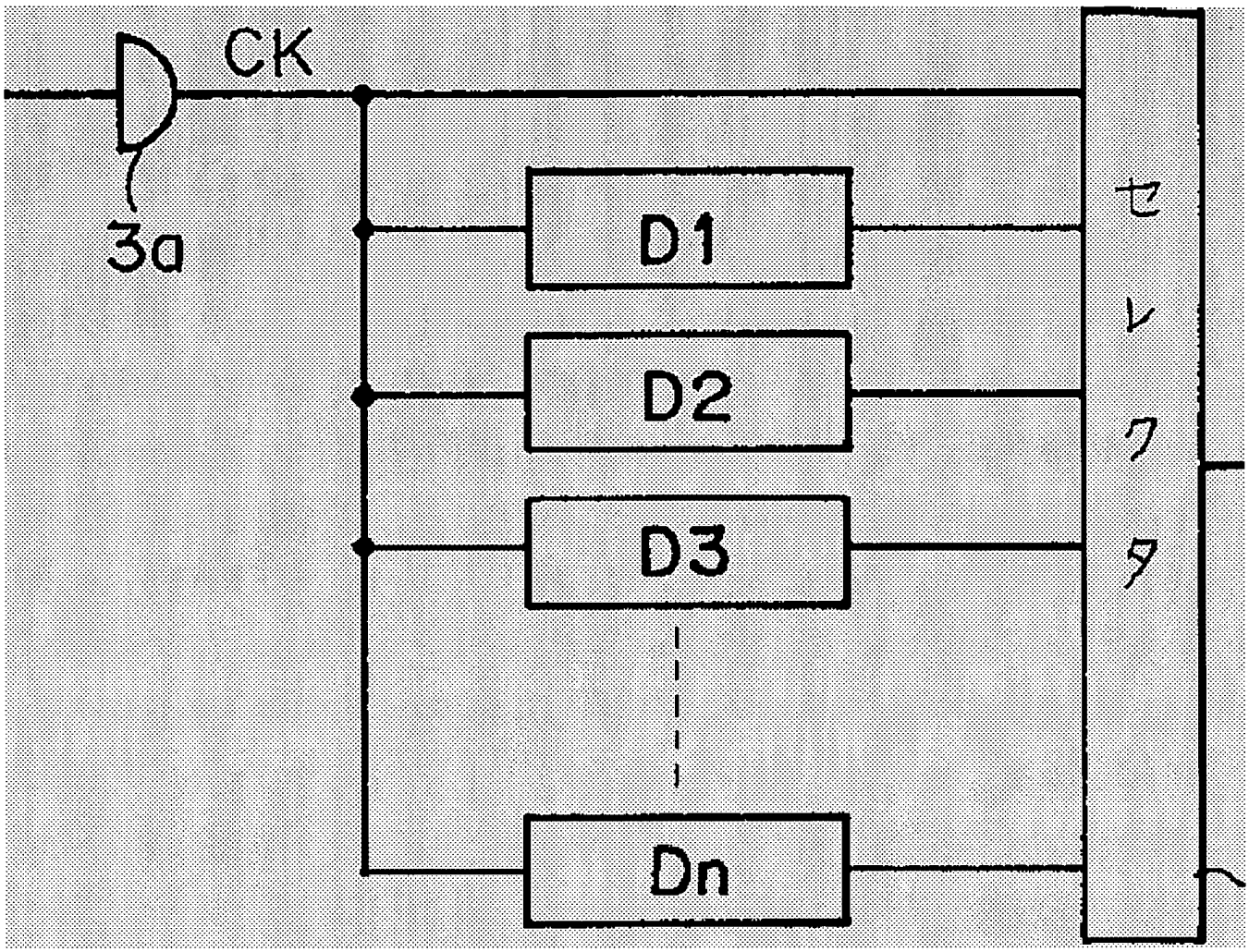
[Drawing 6]



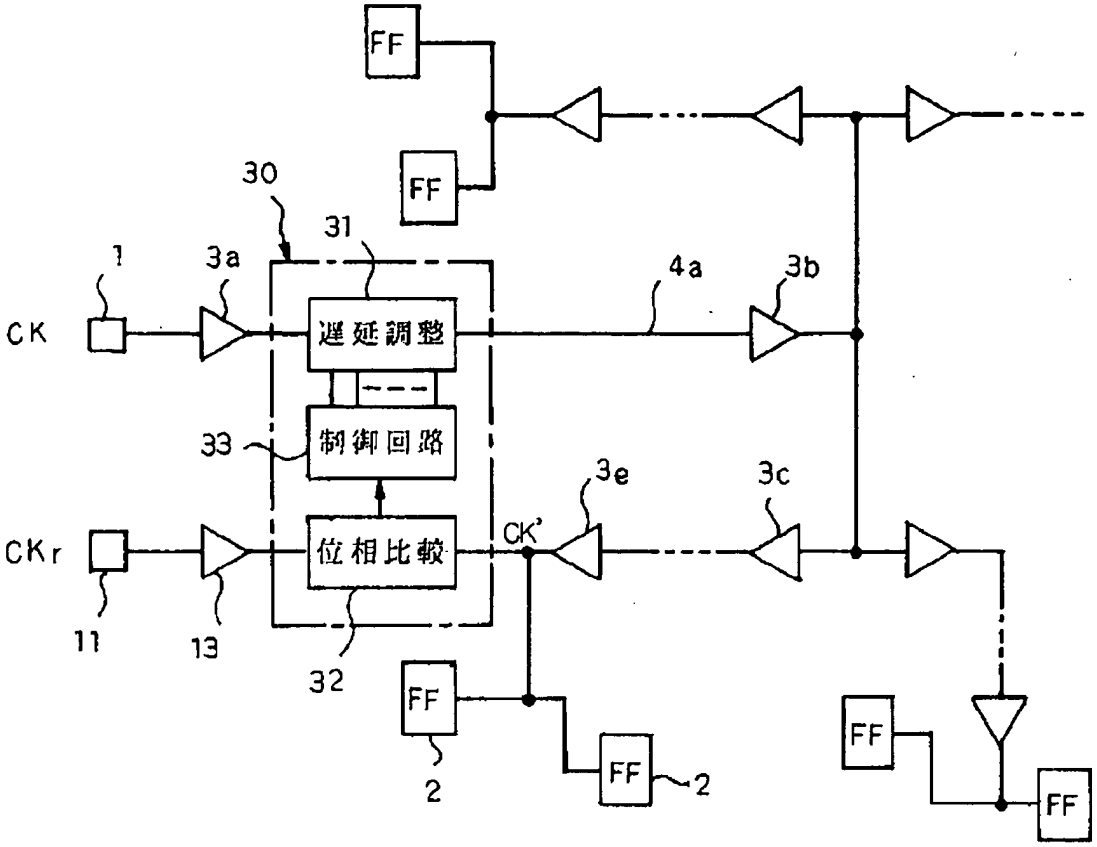
[Drawing 2]



[Drawing 5]



[Drawing 3]



CLAIMS

[Claim(s)]

[Claim 1] The logic integration circuit characterized by being formed so that clock distributive system may branch gradually toward the end circuit of a clock supply place for every block and the load of the buffer circuit of each stage may become the same [being constituted], while clock distributive system including the buffer circuit which the inside of a semiconductor chip was mutually divided into two or more blocks with an almost equal area, and was connected to a clock input terminal and this terminal for every block is established respectively and independently.

[Claim 2] The inside of a semiconductor chip is mutually divided into two or more blocks with an almost equal area. And while clock distributive system including the buffer circuit and phase adjustment circuit which were connected to a clock input terminal and this terminal for every block is constituted independently, respectively The logic integration circuit characterized by being constituted so that the clock signal for the reference supplied from the outside and the clock signal supplied to an end circuit through the above-mentioned clock distributive system may return to the above-mentioned phase adjustment circuit and phase adjustment of a clock signal may be performed.

[Claim 3] The logic integration circuit characterized by being constituted so that the clock signal for reference supplied from the outside and the clock signal inputted from the common clock terminal may be supplied to the above-mentioned phase adjustment circuit and phase adjustment of a clock signal may be performed, while the clock distributive system which the inside of a semiconductor chip be mutually divided into two or more blocks with an almost equal area, and include a clock buffer circuit and a phase adjustment circuit for every block be constituted independently, respectively.